**IN THE SPECIFICATION:**

Please replace paragraph 39 with the following amended paragraph:

[0039] Though not illustrated in FIGURE 1, the DSP 100 has an overall memory architecture that ~~100~~ is typical of conventional DSPs and microprocessors. That is, its registers are fast but small; its instruction and date caches (contained respectively in the PFU 110 and the LSU 140) are larger, but still inadequate to hold more than a handful of instructions or data; its local instruction memory and data memory ~~122~~ are larger still, but may be inadequate to hold an entire program or all of its data. An external memory (not located within the DSP 100 itself) is employed to hold any excess instructions or data.

Please replace paragraph 43 with the following amended paragraph:

[0043] The ISU 120 contains an instruction decode block *isu_fd_dec* 210; a conditional execution logic block *isu_cexe* 220; a program counter (PC) controller *isu_ctl* 230; an instruction queue (containing an instruction queue control block *isu_queue_ctl* 240 and an instruction queue block *isu_queue* 250); an instruction grouping block *isu_group* 260; a secondary decode ~~control~~ logic block *isu_2nd_dec* 270; and a dispatch logic block *isu_dispatch* 280.

Please replace paragraph 49 with the following amended paragraph:

[0049] The secondary decode ~~control~~ logic block *isu_2nd_dec* 270 provides additional instruction decode logic 271 for the GR, RD, M0 and M1 stages of the pipeline. The main function of the additional instruction decode logic 271 is to provide additional information from each

instruction's opcode to *isu_group* 260. The instruction decoders in *isu_2nd_dec* 270 are the same as those employed in the additional decode logic 212 of *isu_fd_dec* 210.

Please replace paragraph 57 with the following amended paragraph:

[0057] A return PC unit 300 contains FIFO control logic 310, the return PC FIFO queue 233 ~~234~~ and staging registers 340. The FIFO control logic 310 is responsible for controlling the operation of the return PC unit 300 as a whole. The return PC FIFO queue 233 ~~234~~ and staging registers 340 cooperate with each other to form return PC storage. The staging registers 340 allow the return PC value to be drawn from the return PC FIFO 233 ~~234~~ and to track its corresponding return instruction as it moves through stages in the pipeline.

Please replace paragraph 59 with the following amended paragraph:

[0059] Under control of the FIFO control logic 310, a return PC value equaling the current value of the PC, plus one, is loaded into the return PC FIFO queue 233 ~~234~~ (by way of a *currentpc_p1_fd* bus ~~302~~). The current value of the PC is offset by one, because that is the size of the last instruction executed in the main routine (or calling subroutine) before the *call* instruction routine. (Instructions can be of variable length, e.g., one or two words, or more.) When that value is eventually loaded into the PC (upon execution of a corresponding return instruction), the PC then points to the correct instruction to be executed.

Please replace paragraph 60 with the following amended paragraph:

[0060] Since the F/D stage of the pipeline of the DSP 100 of FIGURE 1 is capable of decoding a maximum of three call instructions prior to grouping in the GR stage, the return PC FIFO queue 233 ~~234~~ has three slots. When the return instruction corresponding to a return PC value contained in one of the slots actually enters the pipeline, that slot is selected by way of the multiplexer 320, causing the return PC value to move into the staging registers 340. As the corresponding return instruction moves through the various stages of the pipeline (RD, AG, M0, M1, EX), the return PC value moves through the corresponding RD, AG, M0, M1 and EX staging registers 340.